Capacitance compact modelling of four-terminal graphene FETs preserving charge conservation: A circuit-oriented device model benchmark

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Abstract

Experimental research into GFETs has rapidly increased in the past few years, mainly because of the potentially achievable extremely high-speed performance. However, there has been little exploration on the physical behavior of these devices under dynamic conditions. Previous examinations [1-2] have either been incomplete or have applied conventional (silicon based), and therefore inappropriate, assumptions regarding device behavior to the analysis. Such models, when applied to GFETs, may incorrectly interpret and predict the frequency performance of these devices.

Most circuits operate under time-varying terminal voltage excitation of the constituting devices. The dynamic operation is affected by the capacitive effects of the device, rendering indeed essential for eventual circuit design to derive reliable compact models encompassing such capacitive effects. The most common approach to silicon-device capacitive modeling is the Meyer model, which is based upon non conservation of the charge and assumes the intrinsic capacitances as 2-terminal lumped capacitances [3]. Although it exhibits problems with some circuits (e.g. DRAMs and switched capacitor filters) this compact model is widely used because of its simplicity and fast computation. Most of the GFET compact models hitherto found in the literature are directly based upon such Meyer model. The question arises on whether Meyer capacitance model is also suitable for GFETs.

In this framework, a compact capacitance-model for double-gate four-terminal GFETs derived from the Ward-Dutton's linear charge partition scheme, which preserves the charge conservation, has been recently developed [4]. The model has been built from a field-effect model and drift-diffusion carrier transport. Using this novel model as a basis, explicit closed-form expressions for the 9 independent capacitances (16 capacitances in total: 4 self-capacitances and 12 intrinsic capacitances) are presented in this paper covering continuously all the operation regions (see Fig. 1, as an illustrative example). Additionally, they have been implemented in Verilog-A, a language suited to circuit simulators. To assess the impact of the new charge-conservation capacitive model of GFETs upon circuit performance, this capacitance-model [4] is benchmarked at the circuit level against an alternative Meyer-based capacitance-model [5] and the correspondent conclusions are drawn.

References

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Figures

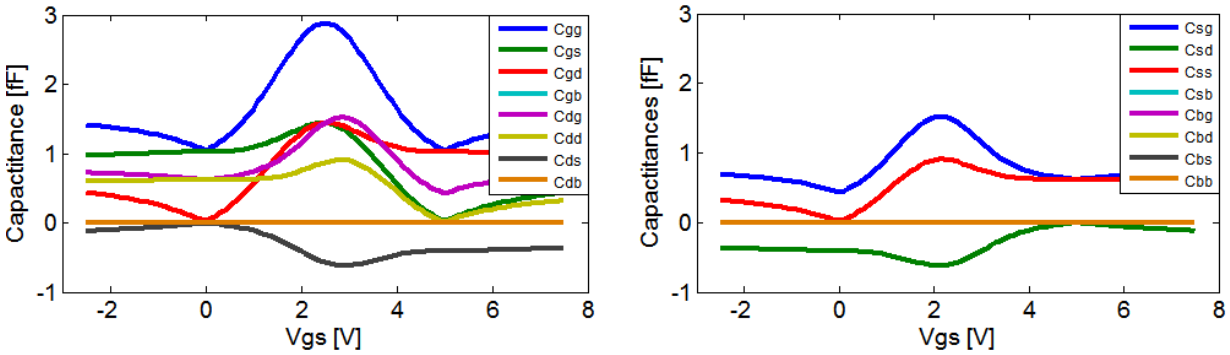

FIG. 1.- GFET capacitances versus the gate bias for the device considered in Ref. [6] under V_{ds} = 5V. Notice that capacitances C_{gb}, C_{db}, C_{sb}, C_{bg}, C_{bd}, C_{bs}, C_{bb} are almost negligible because the bottom oxide thickness is much larger than the top oxide.

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